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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,950	02/02/2001	Jiangnan Chen	CE08674R	1513

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EXAMINER
ABRAHAM, ESAW T

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/775,950	CHEN ET AL.	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims **1 to 19** are presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for domestic priority under 35 U.S.C. 119 (e) (provisional application # 60/223,548) filed on 08/05/2000.

Claim objections

3. Claim 7 objected to because of the following informalities:

Please change the phrase "a input device" to ----an input device---- in claim 7 line 2.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-6 are rejected under 35 U.S.C. 101 because the claimed invention are directed to algorithm not embedded in computer readable medium. For example, the steps of writing address locations of data elements sequentially by row into a matrix having a predetermined number of rows having corresponding row indexes and a second predetermined number of columns, bit reversing the row/column indexes and shifting bit storage locations are only directed to mathematical algorithms rather than limited to practical applications.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 7-**19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Eroz et al. (U.S. PN: 6,333,197).

As per claims **7, 14 and 15,** Eroz et al. teach interleavers implemented by the interleaver (see fig. 2, element 16) is a two-dimensional block interleaver (or interleaver matrix) is a number rows and a number of columns whereby an input data are written into the interleaver matrix row by row and then row and column permutations are performed to randomize data positions wherein the data are then read out column by column (see col. 9, lines 2-10). Further, Eroz et al. teach an input position l=C.multidot.i+j, a corresponding output interleaved position given by mathematical formula I(l)=R.multidot..pi..sub.i (j)+.rho.(i), wherein .pi..sub.i s a column permutation applied to

data in row i and wherein .rho. is bit-reversed indexing, which is especially simple to implement and requires no additional parameter storage in the memory of the interleaver (16) (see col. 9, lines 11-17). Eroz et al. **do not explicitly** teach a controller configured to bit reverse row and column indexes. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made, such controllers are required in order to perform write and read operation for forward or backward (bit reversing) operations. **Accordingly,** it would have been obvious to one ordinary skill in the art to have included a controller because such controllers would have required in order to send signals or data in a forward or backward direction, following predetermined order within the error correction system.

As per claims **8-9, 12, and 16-19,** Eroz et al. teach all the subject matter in claims 1, 7, and 13 including a process of reordering a sequence of symbols or bits in a predetermined manner whereby an interleaver size is equal to the size of the sequence and turbo interleavers are interleavers used in the construction of turbo codes wherein a turbo code built as a parallel concatenation of two constituent recursive convolutional codes, serves to re-order an input data sequence in a pseudo-random fashion prior to an encoding by a second of the constituent codes and as a result, separate encoding produced by the two constituent encoders are largely uncorrelated, which property allows them to be combined by a turbo encoder (see col. 1, lines 15-30). Further, Eroz et al. teach interleavers of size 2.sup.m are constructed, for any window of size 2W, W an integer, there is at most W indices that must be pruned in order to obtain an interleaver of size N wherein 2.sup.m-<N.ltoreq.2.sup.m (see col. 12 lines 10-19). Eroz et al. **do not explicitly** teach setting the numbers of rows and columns to 2^m and 2^n, where the

value m and n are set to 2^{m+n} is equal to N number of bits. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made, setting the numbers of rows and columns to predetermined number of bits is required to perform a process of interleaving or re-ordering a sequence of symbols (bits) and setting the numbers of rows and columns to obtain different values depends up to the designers' choice. **Accordingly,** it would have been obvious to one ordinary skill in the art to determine and set numbers of rows and columns to obtain different values because such methods would have been required in order to facilitate operations of matrix equation.

As per claims **10 and 11,** Eroz et al. teach all the subject matter claimed in claims 1 and 7 including a method of re-ordering the rows according to a bit reversal on row index whereby the contents of the resulting permuted and re-ordered matrix, or interleaver matrix, are read out column by column to an encoder as in the case of a block interleaver (see col. 11, lines 53-67).

As per claim **13,** Eroz et al. in figure 2 disclose a digital communication system comprising a turbo coder (see element 10), an interleaver (see element 16) whereby the interleaver comprising "two-dimensional permutations" including computing the "two-dimensional permutations", further comprising: writing the indexed data into an Interleaver matrix having one or more rows in each of two dimensions; permuting the indexed data in one or more rows in at least one of the two dimensions to produce "constituent permutations"; reading out the data from the Interleaver matrix; selecting one of the basic Interleavers for use in encoding based upon a desired Interleaver length L; providing an Interleaver device for interleaving blocks of indexed data, the interleaver device further comprising a memory device for storing descriptions of the

basic interleavers; and storing the descriptions in the memory device (see col. 2, lines 1-30). Further, Eroz et al. teach a permutation related to a bit-reversal indexing (see col. 6, lines 33-44). Furthermore, Eroz et al. in figure 1 teach a turbo decoder (see element 132) and then the fixed length data units passed to the turbo coder (see element 108) which uses an interleaver to pseudo-randomize the input between two concatenated encoders and encodes the fixed length data units (data streams) and sends encoded data units (data streams) and further the turbo decoded by turbo decoder 132 through a concatenation of decoders and an interleaver using feedback from each other decoder to decode information from the received burst (see col. 4, lines 25-37). Eroz et al. **do not explicitly** teach shifting bit storage locations of one or more predetermined numbers of rows and columns. **However,** Eroz et al. teach that coded bits output the current encoding by shifting the contents of the shift registers (see figure 2, elements 18, 21, 22) once to prepare for a next encoding step (see col. 5, lines 25-65) which the methods of shifting the contents (bits) of shift registers taught by Eroz et al. are similar to the applicants' method. **Therefore,** it would have been obvious at the time the invention was made to one of ordinary skill in the art to shift bit storage locations. **This motivation** would have been obvious to one ordinary skill in the art at the time the invention was made because one of ordinary skill in the art would employ the process of shifting bit storages in order to facilitate utilization of flexible and efficient memory configurations.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN:	6,493,815	Kim et al.
US PN:	6,314,534	Agrawal et al.
US PN:	6,304,991	Rowitch et al.
US PN:	5,996,104	Herzberg, Hanan
US PN:	6,598,202	Kim et al.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Art unit: 2133

Guy J. Lamarre for

Albert DeCady
Primary Examiner